This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously presented): An integrated circuit, comprising:

a reconfigurable interconnect portion;

a data processing portion coupled to the reconfigurable interconnect portion, the data processing portion configured to provide a bit pattern to the reconfigurable interconnect portion to load a configuration of the reconfigurable interconnect portion; and

a storage unit coupled to the data processing portion, the storage unit including a configuration bit look-up table,

wherein the data processing portion is configured to extract a set of bits from the configuration bit look-up table to map a common plurality of inputs of the reconfigurable interconnect portion to a plurality of outputs of the reconfigurable interconnect portion.

Claim 2 (previously amended): The integrated circuit of claim 1, wherein the integrated circuit includes a second reconfigurable interconnect portion, and the configuration bit look-up table is configured to allow the data processing portion to extract a first set of configuration bits representing the bit pattern and to extract a second set of configuration bits representing a second bit pattern to load a second configuration of the second reconfigurable interconnect portion, wherein the second set is a subset of the first set.

Claim 3 (original): The integrated circuit of claim 1, wherein the reconfigurable interconnect portion comprises a switching matrix.

Claim 4 (previously amended): The integrated circuit of claim 1, wherein reconfigurable interconnect portion comprises a multiplexer.

Claim 5 (original): The integrated circuit of claim 3, wherein the switching matrix includes a control signal input configured to select between two inputs to connect to an output.

Claim 6 (original): The integrated circuit of claim 1, wherein the reconfigurable interconnect portion comprises a pair of transistors.

Claim 7 (original): The integrated circuit of claim 1, wherein the reconfigurable interconnect portion comprises a plurality of memory elements, each memory element connected to at least one switch of the reconfigurable interconnect portion.

Claim 8 (original): The integrated circuit of claim 1, wherein the bit pattern is derived from the configuration bit look-up table.

Claim 9 (original): The integrated circuit of claim 1, wherein the configuration bit look-up table comprises a plurality of rows of configuration bits.

Claim 10 (original): The integrated circuit of claim 9, wherein the storage unit is coupled to the data processing portion by a plurality of address lines for accessing the rows of configuration bits stored within the storage unit.

Claim 11 (original): The integrated circuit of claim 10, wherein the storage unit further comprises programming instructions configured for accessing the configuration bit look-up table, wherein the programming instructions are further configured for extracting a subset of configuration bits from the configuration bit look-up table.

Claim 12 (previously presented): The integrated circuit of claim 1, wherein the data processing portion is configured to map a first input of the common plurality of inputs of the reconfigurable interconnect portion to a first output of the plurality of outputs of the reconfigurable interconnect portion in response to a first command.

Claim 13 (previously presented): The integrated circuit of claim 12, wherein the data processing portion is configured to map a second input of the common plurality of inputs of the reconfigurable interconnect portion to a second output of the plurality of outputs of the reconfigurable interconnect portion in response to the first command.

Claim 14 (previously presented): The integrated circuit of claim 12, wherein the data processing portion is configured to map a second input of the common plurality of inputs of the reconfigurable interconnect portion to a second output of the plurality of outputs of the reconfigurable interconnect portion in response to a second command.

Claim 15 (original): The integrated circuit of claim 12, further comprising a second reconfigurable interconnect portion, and wherein the data processing portion is configured to map a first input of the second reconfigurable interconnect portion to a first output of the second reconfigurable interconnect portion in response to a second command.

Claims 16-34 (canceled)

Claim 35 (previously presented): An integrated circuit comprising a reconfigurable interconnect portion and a storage unit coupled to the reconfigurable interconnect portion, wherein the storage unit stores a look-up table for use in configuring the reconfigurable interconnect portion,

wherein the data processing portion is configured to extract from the look-up table a set of bits to map a common plurality of inputs of the reconfigurable interconnect portion to a plurality of outputs of the reconfigurable interconnect portion.

Claim 36 (previously presented): An integrated circuit, comprising:

a reconfigurable interconnect portion;

a data processing portion coupled to the reconfigurable interconnect portion, the data processing portion configured to provide a bit pattern to the reconfigurable interconnect portion to load a configuration of the reconfigurable interconnect portion; and

a storage unit coupled to the data processing portion, the storage unit including a look-up table,

wherein the look-up table is configured to allow the data processing portion to extract a first set of bits representing the bit pattern and to extract a second set of bits representing a second bit pattern to load a second configuration of a second reconfigurable interconnect portion,

wherein the second set is a subset of the first set,

wherein the extraction of the second set of bits from the look-up table maps a common plurality of inputs of the reconfigurable interconnect portion to a plurality of outputs of the reconfigurable interconnect portion.

Claim 37 (canceled).

Claim 38 (canceled).

Claim 39 (canceled).